SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

A 500W HIGH POWER FACTOR WITH THE L4981A CONTINUOUS MODE IC

The widespread use of passive AC/DC off-line converters causes low power factor and high line current harmonic distortion. To reduce these phenomena and to comply with relevant regulatory agency requirements such as IEC555-2, designers are employing active power factor correction in their off-line SMPS applications. This paper describes a practical, low cost and easy to implement 500W power factor corrected application that employs the L4981A Continuous Mode PFC IC.

INTRODUCTION

Reduction of line current harmonic distortion and improvement of power factor is of great concern to many designers of off-line switched mode power supplies. This concern has been motivated by present and impending regulatory requirements regarding line current harmonics, most notably Standard IEC555-2. The reasons for improving power factor and reducing line current harmonic distortion are well known and understood. Active power factor correction using the boost topology and operating in the continuous inductor current control mode is an excellent method to comply with these requirements and is well accepted in the industry.

This paper will present a practical power factor corrected design for a 500 Watt output and universal mains input application. The detailed derivations of all power, IC biasing and control component values and types will be shown. The evaluation results from an actual working demoboard will be presented as well as several relevant oscillograms.

DESIGN SPECIFICATIONS

The design specifications given below are realized by the implementation of a functional demoboard.

The design target specifications are as follows:

- Universal mains input AC voltage V_{irms} = 88Vac to 264Vac, 60/50Hz
- DC regulated output voltage V_{out} = 400Vdc
- Full load output ripple voltage ΔV_{ripple} = ±8V
- Rated output power P_{out} = 500W
- Maximum output overvoltage V_{omax} = 450V
- Switching frequency f_{sw} = 80kHz
- Maximum inductor current ripple ΔI_L = 23%
- Input power factor PF > 0.99
- Input line current total harmonic distortion <5%

To meet these specifications, the selection of component values and material types is very important. The next sections will describe the component selection criteria along with some critical derivations. For detailed explanations on the controller operation and pin description, refer to Application Note AN628 Designing A High Power Factor Switching Preregulator With The L4981 Continuous Mode [1] and the corresponding Datasheet L4981A/B Power Factor Corrector [2].

POWER COMPONENTS SELECTION

The power component values and types are derived and selected in the next section. Please refer to Figure 2, 500 Watt Demoboard Schematic.

Input Diode Bridge

The input diode bridge, D1, can be a standard slow-recovery type. The selection criteria include the maximum peak reverse breakdown voltage, maximum forward average current, maximum surge current and thermal considerations.

Maximum peak reverse voltage:

$$V_{prv} = V_{irmsmax} \cdot \sqrt{2} \cdot 1.2 \text{ (safety margin)} =$$
$$= 264V \cdot \sqrt{2} \cdot 1.2 = 448V$$

Therefore use a 600V rated diode.

Maximum forward average current:

$$I_{rmsmax} = \frac{P_{OUT}}{V_{rms\,min} \cdot n} = \frac{500}{88 \cdot 0.9} = 6.31A$$

$$I_{fave} = \frac{I_{rmsmax} \cdot \sqrt{2}}{\pi} = \frac{6.31 \cdot \sqrt{2}}{\pi} = 2.84A$$

The thermal considerations require the I_{fave} rating to be significantly higher than the value calculated. The part chosen has a I_{fave} of 25A. Addi-

tionally, a small heatsink is required to keep the case temperature within specification.

Maximum surge current:

There is a significant inrush current at start-up due to the large value bulk capacitor, C6, at the output. There is minimal impedance from the mains to this capacitor, thus at the peak of the input voltage waveform a large inrush current exists. This inrush current can be significantly reduced by some means of current limiting such as an NTC or triac/resistor combination. The input bridge diode's maximum surge current rating must not be exceeded. This demoboard has a low cost and simple NTC for current inrush limiting. The efficiency can be improved by using the triac/resistor scheme, however the cost and complexity increases.

Input Fuse

The input fuse, F1, must open during severe current overloads without tripping during the transient inrush current condition or during normal operation. The fuse must have a current rating above the maximum continuous current (6.3Arms) that occurs at the low line voltage (88V). The fuse chosen for this demoboard has a continuous current rating of 10A/250VAC.

Input Filter Capacitor

The input filter capacitor, C3, is placed across the diode bridge output. This capacitor must smooth the high frequency ripple and must sustain the maximum instantaneous input voltage. In a typical application an EMI filter will be placed between the mains and the PFC circuit. This demoboard does not have the EMI filter except for this input capacitor. However, the evaluation results listed in Table 1 were made with an EMI filter placed between the mains input and the PFC circuit. The design of the EMI filter is not described here. The value of the input filter capacitor can be calculated as follows:

$$Cin > Kr \frac{I_{rms}}{2 \cdot \pi \cdot f_{sw} \cdot r \cdot V_{rms\ min}}$$

$$Cin > 0.25 \cdot \frac{6.31}{2 \cdot \pi \cdot 80k \cdot 0.06 \cdot 88} = 0.59\mu F.$$

Where: Kr is the current ripple coefficient
r = 0.02 to 0.08

The maximum value of this capacitor is limited to avoid line current distortion. The value chosen for this demoboard is 0.68µF.

Output Bulk Capacitor

The choice of the output bulk capacitor, C6, depends on the electrical parameters that affect the filter performance and also on the subsequent application.

Capacitance Value:

The value shall be chosen to limit the output voltage ripple according to the following formula:

Assume low ESR and $\Delta V_{ripple} = \pm 8V$

$$Cout = \frac{P_{out}}{2\pi \cdot 2f \cdot \Delta V_O \cdot V_O} = \frac{P_{out}}{2\pi \cdot 120 \cdot 8 \cdot 400} = 207\mu F$$

The value chosen is 330uf to ensure that the maximum specified voltage ripple is not exceeded.

Although the ESR does not normally affect the voltage ripple, it has to be considered for the power losses due to the line and switching frequency ripple currents. It is important to verify that the low and high frequency ripple currents do not exceed the manufacturer's specified ratings at the operating case temperature. Capacitors may be connected in parallel to decrease the equivalent ESR and to increase the ripple current handling capability.

If a specific hold-up time is required, that is the capacitor has to deliver the supply voltage for a specified time and for a specified dropout voltage, then the capacitor value will be determined by the following equation:

$$Cout = \frac{2 \cdot P_{out} \cdot t_{hold}}{V_{o\ min}^{\ 2} - V_{op\ min}^{\ 2}}$$

Where:

P_{out} is the maximum output power

V_{omin} is the minimum output voltage at max. load

V_{opmin} is the minimum operating voltage before "power fail" detection

t_{hold} is the required hold-up time

Voltage Rating:

The capacitor output voltage rating should not be exceeded under worst case conditions. The minimum voltage rating is calculated as follows:

$V_{cap} > V_{out} + \Delta V_{ripple} + V_{margin} = 400 + 8 + 40 = 448V$

Where: V_{out} is the nominal regulated DC output voltage

ΔV_{ripple} is the ac voltage superimposed on the regulated DC output voltage

ΔV_{margin} is the allowance for tolerances in V_{out} and additional margin before OVP intervention

The capacitor chosen has a voltage rating of 450VDC. The overvoltage trip level of Pin 3 (OVP) must be set below 450VDC.

Power Mosfet

The power mosfet, Q1, is used as the active switch due to its high frequency capability, ability to be driven directly from the controller and availability. The main criteria for its selection include the drain to source breakdown voltage (BVdss), delivered power and temperature considerations.

Voltage Rating:

The power mosfet has to sustain the maximum boosted output dc voltage according to the following equation:

$BV_{dss} > V_{out} + \Delta V_{ripple} + V_{margin} = 400 + 8 + 40 = 448V$

The power mosfet chosen has a BV_{dss} of 500V.

Power Rating:

The main parameters to consider are Rdson and the thermal characteristics of the package and heatsink. The main losses in the power mosfet are the conduction and switching losses. The switching losses can be separated into two quantities, capacitive and crossover losses. The switching losses are dependent on the mosfet current di/dt.

The maximum conduction (on-state) power losses can be calculated according to the following equations:

$$I_{Qrms}max = \frac{P_{out}}{\eta \cdot \sqrt{2}\, V_{irms\ min}} \cdot \sqrt{2 - \frac{16 \cdot \sqrt{2} \cdot V_{irms\ min}}{3\pi \cdot V_{out}}} =$$

$$= \frac{500 / 0.9}{\sqrt{2} \cdot 88} \cdot \sqrt{2 - \frac{16 \cdot \sqrt{2} \cdot 88}{3\,\pi \cdot 400}}$$

$I_{Qrms}max = 5.42A$

$P_{on}max = I_{Qrms}^2 max \cdot R_{(DS)}on\ max = 5.42^2 \cdot 0.54 = 15.86W$

Where:

$I_{Qrms}max$ is the max. power mosfet rms current

$V_{irms}min$ is the min. specified rms input voltage

$R_{(DS)}on\ typ. = 0.27\Omega$ at 25°C at 10A, $V_{GS} = 10V$

$R_{(DS)}on\ max = 0.54\Omega$ at 100°C

The capacitive switching losses at turn-on are calculated as follows:

$$P_{capacitive} = (5 \cdot C_{oss} \cdot V_{out}^{1.5} + \frac{1}{2} C_{ext} \cdot V_{out}^2) \cdot \cdot f_{sw} = 2.7W$$

Where:

$C_{oss} = 650pF$ is the mosfet drain capacitance at 25V

$C_{ext} = 100pF$ is the equivalent stray capacitance of the layout and external parts

The estimated crossover switching losses (turn-on and turn-off) are calculated as follows:

$P_{crossover} = V_{out} \cdot I_{Qrms} \cdot f_{sw} \cdot t_{cr} + Prec =$
$= 400 \cdot 5.42 \cdot 80k \cdot 40ns + 1.5 = 8.43W$

Where:

t_{cr} is the crossover time

P_{rec} is the boost diode recovery power loss contribution

To reduce the turn-off losses in the mosfet, an RCD turn-off snubber has been employed. The capacitor value is calculated as follows:

$$C11 = \frac{I_{Q1pk} \cdot t_{rise}}{\Delta V_{out}} = \frac{8.92 \cdot 40ns}{400} = 892pF$$

Therefore, use C11 = 820pF, 1000VDC rating

The resistors, R23-24, must dissipate the energy stored in the snubber capacitor upon turn-on of the power mosfet. The capacitor must fully discharge during the switching cycle. The time constant of the RC combination is determined as follows:

$$R \leq \frac{1}{10} \cdot \frac{1}{f_{SW} \cdot C11} = 1524$$

The power dissipated in the resistors, R23-24, is calculated as follows:

$$Pdiss = \frac{1}{2} C11 \cdot V_{out}^2 \cdot f_{sw} = \frac{1}{2} \cdot 820pF \cdot 400^2 \cdot \cdot 80k = 5.25W$$

Therefore, use R23 = R24 = 510Ω, 3W rating.

The power mosfet chosen is the SGS-THOMSON Part Number STW20NA50.

This part has a BV_{dss} = 500V, R_{DSon} = 0.27Ω, and is in a TO-247 package. In order to keep the junction temperature at a safe level, the mosfet is attached to an AAVID Heatsink Part Number 61085 with a thermal resistance of 3.0°C/W. This will keep the mosfet junction temperature at a safe level at worst case conditions, low-line input voltage (88V) and full load (500W). The thermal resistance of the heatsink may need to decrease depending upon the ambient temperature, type of enclosure (vented or non-vented) and the method of cooling (natural or forced convection).

Boost Diode

The main criteria for the selection of the boost diode, D2, include the repetitive peak reverse breakdown voltage (V_{rrm}), average forward current (I_{fave}), reverse recovery time (t_{rr}) and thermal considerations.

Voltage Rating:

The voltage rating of the boost diode is determined by the same equation as for the power mosfet. The value chosen is V_{rrm} = 600V.

Current Rating:

The power losses in the boost diode consist of the conduction and switching losses. The switching losses are a function of the reverse recovery time (trr) and output voltage (Vout) . The switching losses are negligible compared to the conduction losses if a suitable ultra fast recovery diode is chosen. The conduction power losses can be calculated as follows:

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{500}{400} = 1.25A$$

$$I_{Drms} = \frac{P_{in}}{\sqrt{2}\, V_{in\ rms\,min}} \sqrt{\frac{16 \cdot \sqrt{2} \cdot V_{in\,rms\,min}}{3 \cdot \pi \cdot V_{out}}} = 3.24A$$

$$P_{cond} = V_{to} \cdot I_{out} + I_{Drms}^2 \cdot R_d = 1.15 \cdot 1.25 + +3.24^2 \cdot 0.043 = 1.89W$$

Where:

V_{to} = 1.15V is the threshold voltage of the diode

R_d = 0.043Ω is the diode differential resistance

The diode must sustain the average output current and also keep the power losses to a minimum in order to keep the diode junction temperature within acceptable limits. The switching losses can be significantly reduced if an ultra-fast diode is employed. Since this circuit operates in the continuous current mode, the mosfet has to recover the boost diode minority carrier charge at turn-on.

Thus, a diode with a small reverse recover time, t_{rr}, must be used. This circuit employs the SGS-THOMSON Turboswitch Diode Part Number STTA806D. This part offers the best solution for the continuous current mode operation due to its very fast reverse recovery time, 25ns typical. This part has a breakdown voltage rating (V_{rrm}) of 600V, average forward current rating (I_{fave}) of 8A and reverse recovery time (t_{rr}) of 25ns.

The diode is attached to the same heatsink as the power mosfet, Q1. The STTA806D is non-isolated thus requiring a thermal insulator with good heat transfer characteristics. The STTA806DI is an isolated package and can be attached directly to the heatsink. Silicone thermal grease may be applied to improve the thermal contact between the diode and heatsink.

Boost Inductor

The boost inductor, T1, design starts with defining the minimum inductance value, L, to limit the high frequency current ripple, ΔI_L. The next step is to define the number of turns, air gap length, ferrite core geometry, size and type for the specified power level. Finally, the wire size and type are determined.

In the continuous mode approach, the acceptable current ripple factor, K_r, can be considered between 10% to 35%. For this design, the maximum specified current ripple factor is 23%. The maximum current ripple occurs when the peak of the input voltage is equal to Vout/2.

$$\Delta I_{Lmax} \frac{V_{out}}{4 \cdot f_{SW} \cdot L} = \frac{400}{4 \cdot 80k \cdot 0.5mH} = 2.50A$$

Occurs at $V_{inpk} = V_{out/2}$ = 200V; V_{inrms} = 141V

$$\Delta I_L = \frac{V_{inpk}\ (V_{out} - V_{inpk})}{V_{out} \cdot f_{sw} \cdot L}$$ For all other input voltages

$$Kr = \frac{\Delta I_L}{2 \cdot I_{Lpk}};\ I_{Lpk} = \sqrt{2} \cdot I_{Lrms} = \frac{\sqrt{2} \cdot P_{in}}{V_{inrms}}$$

The minimum boost inductor value can be calculated as follows:

$$L_{min} = \frac{V_{out}}{4 \cdot f_{sw} \cdot \Delta I_{Lmax}} = \frac{400}{4 \cdot 80kHz \cdot 2.50} = 0.5mH$$

The Table shown below relates the current ripple to the input voltage.

$V_{in\ (rms)}$	$V_{in(peak)}$	$I_{L(rms)}$ $I_{in\ (rms)}$	$I_{L(peak)}$	Current Ripple	K_r
88	124	6.31	8.92	2.13	0.119
120	170	4.63	6.55	2.44	0.186
141	199	3.94	5.57	2.50	0.224
180	255	3.09	4.37	2.31	0.264
200	283	2.78	3.93	2.07	0.263
220	311	2.53	3.58	1.73	0.242
240	339	2.31	3.27	1.29	0.197
264	373	2.10	2.97	0.63	0.106

The number of turns, N, can be calculated according to the following formula:

$$N = \frac{L \cdot I_{Lpk}}{A_{eff} \cdot B\,max} = \frac{0.5mH \cdot 8.92mA}{211 \cdot 10^{-6}\,m^2 \cdot 0.36T} = 59\,Turns$$

Where:

L is the calculated inductance value to limit the ripple current, ΔI_L.

I_{Lpk} is the worst case inductor current occurring at low-line input voltage (88V)

A_{eff} is the effective cross-sectional area of the core

B_{max} is the maximum allowable flux density of the core

The air gap is determined by referring to the magnetic core manufacturer's AL vs. air gap curves.

The air gap needed for the specified inductance, turns and core type is found to be 2.8mm in the center post.

To approximate the minimum core size needed for the conversion, the following equation may be used:

$$Volume \geq K \cdot L\,[I_{Lpk} \cdot (I_{Lpk} + \Delta I_L)]$$

Where K is the specific energy constant that depends on the ratio of the gap length (l_{gap}) and the effective length (l_{eff}) of the core set and the maximum ΔB swing. Practically, K can be estimated as follows:

$$K = 11.5\,\frac{l_{eff}}{l_{gap}} = 11.5 \cdot \frac{114}{2.8} = 468$$

Thus, we have the following calculation for the minimum core set volume in cm^3:

$$Volume \geq 468 \cdot 0.5 \cdot 10^{-3}\,[8.92 \cdot (8.92 + 2.5)] = 23.8\,cm^3.$$

The core chosen for this design is an ETD geometry ferrite core set with the following characteristics:

Core type ETD4916A

Effective core volume = 24.0 cm^3.

Effective magnetic path length = 114 mm

Effective core area = 211 mm^2

Ferrite material is 3C85 or equivalent

Np = 59T Ns = 5T

The ETD geometry has the following advantages:

1. Round center post for ease of winding
2. Commercially available from Philips, Siemens, Thomson, Magnetics, etc..
3. Increased winding area
4. The center leg area is equal to the sum of the areas of the two external legs. The legs are working with the same flux density

The wire size is determined by the maximum copper losses allowed and available winding area. For this design the wire size selected was 30AWG, 30 strand Litz.

An auxiliary winding is used to supply power to the controller. The number of turns was determined experimentally to be 5. The worst case conditions for the auxiliary winding power supply voltage are at low-line input voltage (88V) and full load (500Watts) and at high-line input voltage (264V) and light-load. The auxiliary winding must supply sufficient voltage to prevent turn-off (UVLO) during normal operation and also must not supply excessive voltage causing burn-out of the controller.

CoilCraft Part Number R4849-A meets the above specifications and is available.

IC BIASING AND CONTROL COMPONENTS SELECTION

The IC biasing and control component values are derived and selected in the next section. Please refer to Figure 2, 500 Watt Demoboard Schematic.

Pin 1 P-GND (Power stage ground)

This pin should be connected to the source of the power mosfet, Q1, with a short length and wide copper trace on the printed circuit board to minimize the copper trace resistance and inductance. Refer to Figure 3, 500 Watt Demoboard printed circuit board layout.

Pin 2 IPK (Overcurrent protection input)

In order to obtain a very precise overcurrent protection trip level, R12 and R13 are calculated as follows:

$$I_{aux} = \frac{V_{ref}}{R13} = \frac{5.1}{5.1k} = 1mA$$

$$R12 = \frac{R_{sense} \cdot I_{peak}}{I_{aux}} = \frac{0.033 \cdot 17}{0.001} = 561\Omega$$

Use R12 = 562 ohms, R13 = 5.1k

The peak current threshold is set at 17A and R_{sense} is chosen as 0.033 ohms.

Pin 3 OVP (Overvoltage protection input)

The overvoltage protection trip level is determined by the voltage divider across the output bulk capacitor, C6. The resistor values R11, R21 and R22 are calculated as follows:

$$\frac{R21 + R22}{R11} = \frac{V_{out} + \Delta V_{out}}{V_{ref}} - 1 = \frac{400 + 47}{5.1} - 1 = \frac{909k + 909k}{21k}$$

Where ΔV_{out} = 47V is the maximum overvoltage limit.

The overvoltage limit selection is dependent upon the voltage rating of the output bulk capacitor (450VDC) and the power mosfet (500BVdss). Care must be taken that the level is not set too low, thus causing false tripping of the OVP.

Pin 4 IAC (AC current input)

This pin must be connected through resistors R1 and R2 to the rectified line to drive the multiplier with a current I_{IAC} proportional to the instantaneous line voltage as shown below:

$$I_{IAC}(88V) = \frac{V_{inpk}}{R1 + R2} = \frac{\sqrt{2} \cdot 88}{806k + 806k} = 77\mu A$$

$$I_{IAC}(264V) = \frac{\sqrt{2} \cdot 264}{806k + 806k} = 231\mu A$$

Thus I_{IAC} ranges from 77µA to 231µA. The relationship between I_{IAC} and multiplier output current, Imult, is described in section Pin 8 (MULT-OUT).

Pin 5 CA-OUT (Current amplifier output)

The current amplifier output delivers its signal to the PWM comparator. An external network defines the suitable loop gain to process the multiplier output and the inductor current signals. To avoid oscillation problems, the maximum inductor downslope (Vout/L) must be lower than the oscillator ramp-slope (Vsrp*fsw). The current amplifier high frequency gain can be described as follows:

$$G_{ca} = \frac{R15}{R14} + 1 \leq \frac{V_{srp} \cdot f_{sw} \cdot L}{V_{out} \cdot R_{sense}} = \frac{5.0 \cdot 80k \cdot 0.5m}{400 \cdot 0.033}$$

Where:

V_{srp} = 5.0V is the oscillator ramp peak-peak voltage

G_{ca} is the current amplifier gain

f_{sw} = 80kHz is the switching frequency

R_{sense} = 0.033Ω is the parallel combination of R30-32

Thus, use R14=R16=2.7k, and R15=36K.

To define the value of the compensation capacitor, C9, it is useful to consider the open loop current gain, defined by the ratio of the voltage across the sense resistor and the current amplifier output voltage. The crossover frequency is given by the following equation:

$$f_c = \frac{f_{sw}}{2 \cdot \pi} = \frac{80k}{2 \cdot \pi} = 12.7kHz$$

To ensure a good phase margin, the zero frequency, fz, should equal approximately $f_c/2$.

$$f_z = \frac{f_{sw}}{4\pi} = \frac{1}{2 \cdot \pi \cdot C9 \cdot R15} \text{ therefore,}$$

$$C9 = \frac{2}{R15 \cdot f_{sw}} = 692pF$$

Use C9 = 680pF

Pin 6 LFF (Load feed-forward input)

This pin allows the modification of the multiplier output current proportionally to the load in order to improve the load transient response time. This function is not used in this circuit and the pin is connected to VREF.

Pin 7 VRMS (Voltage input)

This function is very useful for universal input mains applications to compensate the gain variation related to the input voltage change. This pin is connected through an external network to the rectified line input. The best control is achieved when the VRMS voltage level is in the range of 1.5 to 5.5V.

To avoid the rectified mains line ripple (2f), a two pole low-pass filter is realized with R3-R6 and C1-2. The lowest pole is set near 3Hz and the highest pole near 13 Hz to reduce the gain to -80dB at 100 Hz.

$$V_{rmspin7} = \left(\frac{R3}{R3 + R4 + R5 + R6} \right) V_{rmsline}$$

$$f_{pole1} = \frac{1}{(R5 + R6) \cdot C2} = 3.66Hz$$

$$f_{pole2} = \frac{1}{R4 \cdot C1} = 12.6Hz$$

Where:

R3 = 33kΩ, R4 = 360kΩ, R5 = R6 = 620kΩ, C1 = C2 = 220nF

At 88 Vrms, Vpin7 = 1.78 Vrms

At 264 Vrms, Vpin7 = 5.33 Vrms

Gain at 2f (100Hz) = -80dB

For single mains operation, this pin can be connected directly to Vref (pin 11) or to ground and the RC network can be removed. If connected to ground, the Vrms multiplier input is clamped at 1.5V.

Pin 8 MULT-OUT (Output of the Multiplier)

This pin delivers the current Imult that is used to fix the reference voltage for the current amplifier. Pin 8 is connected through R14 to the negative side of the sense resistor, R30-32, to sum the ($I_L \cdot R_s$) and the ($I_{mult} \cdot R14$) signals, where I_L is the inductor current. The sum is the error voltage signal at the current amplifier non-inverting input.

The multiplier output current is determined by the equation given below:

$$I_{mult} = 0.37 \cdot I_{AC} \cdot \frac{(V_{va-out} - 1.28V) \cdot (0.8 \cdot V_{lff} - 1.28V)}{V_{rms}^2} =$$

$$= I_{IAC} \cdot \frac{(V_{va-out} - 1.28V)}{V_{rms}^2}$$

Where:

$V_{va\text{-}out}$ = Error amplifier output voltage range

$V_{lff} = V_{ref} = 5.1V$ if not used for load feed-forward

V_{rms} = Voltage at pin 7

I_{IAC} = Input current at pin 4

To optimize the multiplier biasing for each application, the relationships between Imult and other input signals are reported in the Designing A High Power Factor Switching Preregulator With The L4981 Continuous Mode Application Note [1], Figures 13a-13h.

Pin 9 ISENSE (Current amplifier inverting input)

This pin is the current amplifier inverting input. It is externally connected to the network described at CA-OUT (pin 5). Note that R14=R16=2.7k have the same value because of the high impedance feedback network.

The sense resistors, R30-R32, have a combined resistance of 0.033 ohms. The low value is chosen to minimize the power losses since the total inductor current flows through this resistor. The value must be large enough to provide a good signal to noise ratio signal to the current amplifier.

Pin 10 SGND (Signal ground)

This pin should be connected close to the reference voltage filter capacitor (C7). Refer to Figure 3, 500 Watt Demoboard printed circuit board layout.

Pin 11 VREF (Voltage reference)

An external capacitor filter of 1uF, C7, should be connected from pin 11 (Vref) to ground. This reference voltage of 5.1V is externally available and can deliver up to 10mA for external circuit needs such as the fast start-up power supply circuit as described in Pin 19.

Pin 12 SS (Soft start)

This feature avoids current overload through the power mosfet during the ramp-up of the output boosted voltage. An internal switch discharges the capacitor if an output overvoltage (OVP) or a VCC undervoltage (UVLO) is detected. The voltage at the soft-start pin acts on the output of the error amplifier and the soft start time is calculated as follows:

$$t_{ss} = C_{ss} \frac{V_{va-out}}{I_{ss}} = 1\mu F \frac{5.1V}{100\mu A} = 51ms$$

Where:

C_{ss} = C8 = 1µF

$V_{va\text{-}out}$ = 5.1V is the typical error amplifier voltage swing

I_{ss} is the internal soft start current generator

Pin 13 $V_{va\text{-}out}$ (Error amplifier output)

To ensure system stability, the compensation network must be designed with sufficient phase margin. Additionally, the system must not regulate the twice mains frequency output ripple voltage in order to avoid line current distortion. The compensation capacitor, C10, can be calculated as follows:

$$C_{10} > \frac{1}{4 \cdot \pi \cdot f_{mains} \cdot (R9 + R10) \cdot G_{ea}} = K_a \frac{\Delta V_{out}}{(R9 + R10)}$$

Where:

R9 + R10 are the resistors from the output voltage feedback resistor divider

G_{ea} is the small signal gain of the error amplifier

ΔV_{out} is the maximum output voltage ripple

$K_a = \frac{1}{60}$ for 50 Hz and $\frac{1}{72}$ for 60 Hz mains frequency

$C_{10} > \frac{1}{60} \cdot \frac{8}{824k} = 162nF$, therefore use standard value 220nF

The voltage open loop gain contains two poles at the origin, causing stability problems. This can be avoided by shifting the error amplifier pole from the origin to near the crossover frequency. This can be accomplished by placing a resistor, R19, in parallel with the compensation capacitor, C10. The crossover frequency is calculated as follows:

$$f_c = \sqrt{\left(\frac{P_{out}}{V_{out} \cdot \Delta V_{ea} \cdot 2\pi \cdot C_{out}}\right)\left(\frac{1}{2\pi \cdot (R9 + R10) \cdot C10}\right)} =$$

$$= \sqrt{\left(\frac{500}{400 \cdot 3.82 \cdot 2\pi \cdot 330\mu F}\right)\left(\frac{1}{2\pi \cdot 824k \cdot 220nF}\right)} = 11.77Hz$$

$$R19 \geq \frac{1}{2\pi \cdot f_c \cdot C10} = 83.4k$$

Use R19 = 120k to increase error amplifier dc gain.

Pin 14 VFEED (Error amplifier input)

This pin is the error amplifier inverting input. This pin is connected to the resistor divider connected across the boosted output voltage to provide regulation. The boosted output voltage is specified at 400VDC. The resistor divider network is calculated as follows:

$$\frac{R9 + R10}{R20} = \frac{824k}{10.6k} = \frac{V_{out}}{V_{ref}} - 1 = \frac{400}{5.1} - 1$$

Use R9 = R10 = 412k

Pin 15 P-UVLO (Programmable supply undervoltage threshold)

This pin may be used to modify the turn-on and turn-off power supply thresholds. This circuit does not employ this feature and the pin is left floating. The typical turn-on threshold is 15.5V and the turn-off threshold is 10V.

Pin 16 SYNC (In/Out synchronization)

This function allows for synchronization in master or slave mode with other circuits in the system. This demoboard does not use this function and the pin is left floating.

Pin 17 ROSC (Oscillator resistor)

Pin 18 COSC (Oscillator capacitor)

These pins determine the oscillator frequency of the circuit. A resistor, R17, is connected from pin 17 to ground. A capacitor, C4, is connected from pin 18 to ground. The operating frequency is calculated as follows:

$$f_{SW} = \frac{2.44}{R_{osc} \cdot C_{osc}} = \frac{2.44}{30.1k \cdot 1n} = 80kHz \text{ approx.}$$

Pin 19 VCC (Supply voltage input)

The IC must be supplied with a very low current, 0.3mA typical, during start-up. The turn-on threshold is 15.5V typical with 5.5 Volts typical of hysteresis. The start-up current is provided by the resistor/capacitor network driven off the rectified line voltage. A fast start-up circuit is employed to quickly turn on the IC and reduce power consumption in the start-up resistor, R28. The capacitor, C12, has a value of 220uF to ensure sufficient hold-up time to allow the auxiliary winding to provide voltage after initial start-up. The fast start-up is realized with Q2, Q3, R25, R26, R27, R28, D5 and C12. The fast start-up circuit is turned-off when the controller turn-on threshold is reached and Vref forward biases Q2, pulling the gate of Q3 to ground.

The auxiliary winding on the main boost inductor provides the normal operating voltage for the controller. The voltage induced on this winding is rectified by diodes D7-D10. Resistor R29 provides current limiting and zener D6 regulates the supply voltage to 18 Volts.

Pin 20 GDRV (Gate driver output)

The output of this pin is internally clamped at 15V to prevent breakdown of the power mosfet gate oxide. A resistor, R18, of 15Ω is placed in series with the gate of the power mosfet to avoid overshoot and limit the di/dt of the switch. A 1N4148 diode, D3, is connected to the gate to provide fast turn-off of the power mosfet.

EVALUATION RESULTS

The 500W demoboard has been evaluated for the following parameters: PF (power factor), % THD (percent total harmonic distortion), H3..H7 (percentage of current's nth harmonic amplitude), Vout (output voltage) and efficiency (n). The test configuration and test results are shown below:

Test Set-Up and Equipment

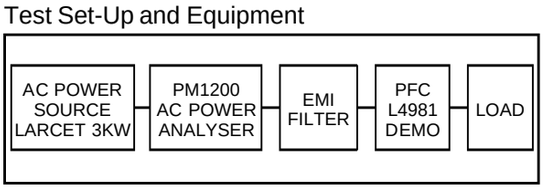


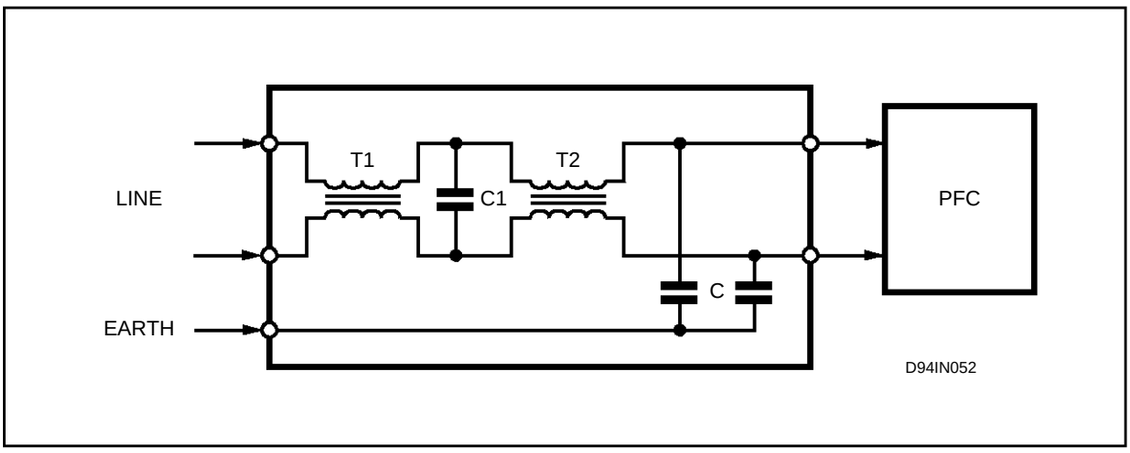
Table 1: 500W Demoboard Evaluation Results

V_{in}	f	P_i	PF	THD	H3	H5	H7	V_{out}	P_o	η
(V_{rms})	(Hz)	(W)		(%)	(%)	(%)	(%)	(V)	(W)	(%)
88	60	560	99.9	2.9	1.3	1.7	1.2	402	490	87.5
110	60	543	99.9	2.8	1.4	1.8	1.3	403	492	90.6
220	50	525	99.8	3.3	1	2.4	1.1	406	499	95.1
270	50	523	99.8	3.4	1	2.6	1.1	408	504	96.3

EMI/RFI FILTER

The harmonic content measurement was made with the EMI/RFI filter interposed between the AC source and the demoboard under test, while the efficiency has been calculated without the filter contribution.

Figure 1: EMI/RFI Test Filter



Part List of the Figure 2.

Part Des.	Description	Vendor's Part #
Fuse F1	Fuse, 3AG Fast Acting 10A, 250VAC	Digi-Key #F127-ND
Fuse Clip	3AG Fuse Clips	Digi-Key #F048-ND
C1	Met. Poly. Film Cap., 0.22µF, 100V Panasonic ECQ-E1224KF	Digi-Key #EF1224
C2	Met. Poly. Film Cap., 0.22µF, 100V Panasonic ECQ-E1224KF	Digi-Key #EF1224
C3	Met. Poly. Film, .68uF, 250VAC, Panasonic ECQU2A684MV	Digi-Key #P4615-ND
C4	Polyester Cap., .001µF, 50V, Panasonic ECQ-B1H102JF	Digi-Key #P4551-ND
C5	Polyester Cap., .012µF, 50V Panasonic ECQ-B1H123JF	Digi-Key #P4583-ND
C6	Alum. Electrolytic Cap., 330µF, 450VDC, 85 Deg. C	Digi-Key#P6443-ND
C7	Electrolytic Cap., 1.0µF, 63V, Panasonic ECE-A1JU010,85Deg C	Digi-Key #P6275-ND
C8	Electrolytic Cap., 1.0µF, 63V, Panasonic ECE-A1JU010,85Deg C	Digi-Key #P6275-ND
C9	Polyester Cap. 680pfd., 50V, Panasonic ECQ-B1H681JF	Digi-Key # P4580-ND
C10	Met. Poly. Film Cap., 0.22µF, 100V Panasonic ECQ-E1224KF	Digi-Key #EF1224
C11	Ceramic Capacitor, 820pfd.,1000VDC	Digi-Key #P4127-ND
C12	Electrolytic Cap., 220µF, 25V,Panasonic ECE-A1EU101,85Deg C	Digi-Key #P6240-ND
D1	Diode Bridge, 600V, 25A	Digi-Key #MB256-ND
D2	STTA806D/DI,, 600V, 8A, Isolated TO220AC Package	SGS-THOMSON STTA806D/DI
D3	Switching Diode, 1N4148, 100V	Digi-Key #1N4148CT-ND
D4	Fast Recovery Diode, STTB406, 600V, 4A	SGS-THOMSON STTB406
D5	Zener Diode, 22V, 1/2W, DO-35 Package	Digi-Key #1N5251BCT-ND
D6	Zener Diode, 18V, 1/2W, DO-35Package	Digi-Key #1N5248BCT-ND
D7	Fast Recovery Rectifier Diode, 100V, 1.5A	SGS-THOMSON BYW-100-100
D8	Fast Recovery Rectifier Diode, 100V, 1.5A	SGS-THOMSON BYW-100-100
D9	Fast Recovery Rectifier Diode, 100V, 1.5A	SGS-THOMSON BYW-100-100
D10	Fast Recovery Rectifier Diode, 100V, 1.5A	SGS-THOMSON BYW-100-100
R1	Metal Film Res., 806K, 1/4W, 1%	Digi-Key #806KXBK-ND
R2	Metal Film Res., 806K, 1/4W, 1%	Digi-Key #806KXBK-ND
R3	Carbon Film Res., 33K, 1/4W, 5%	Digi-Key #33KQBK-ND

Part List of the Figure 2 (continued)

Part Des.	Description	Vendor's Part #
R4	Carbon Film Res., 360k, 1/4W, 5%	Digi-Key #360KQBK-ND
R5	Carbon Film Res., 620k, 1/4W, 5%	Digi-Key #620KQBK-ND
R6	Carbon Film Res., 620k, 1/4W, 5%	Digi-Key #620KQBK-ND
R9	Metal Film Res., 412k, 1/4W, 1%	Digi-Key #412KXBK-ND
R10	Metal Film Res., 412k, 1/4W, 1%	Digi-Key #412KXBK-ND
R11	Metal Film Res., 21k, 1/4W, 1%	Digi-Key #21.0KXBK-ND
R12	Metal film Res., 562, 1/4W, 1%	Digi-Key #562XBK-ND
R13	Metal Film Res., 5.11k, 1/4W, 1%	Digi-Key #5.11KXBK-ND
R14	Carbon Film Res., 2.7k, 1/4W, 5%	Digi-Key #2.7KQBK-ND
R15	Carbon Film Res., 36k, 1/4W, 5%	Digi-Key #36KQBK-ND
R16	Carbon Film Res., 2.7k, 1/4W, 5%	Digi-Key #2.7KQBK-ND
R17	Metal Film Res., 30.1k, 1/4W, 1%	Digi-Key #30.1KXBK-ND
R18	Carbon Film Res., 15 ohms, 1/4W, 5%	Digi-Key #15QBK-ND
R19	Carbon Film Res., 120k, 1/4W, 5%	Digi-Key #120KQBK-ND
R20	Metal Film Res., 10.7k, 1/4W, 1%	Digi-Key # 10.7KXBK-ND
R21	Metal Film Res., 909k, 1/4W, 1%	Digi-Key #909KXBK-ND
R22	Metal Film Res., 909k, 1/4W, 1%	Digi-Key #909KXBK-ND
R23	Metal Oxide Resistor, 510 ohms, 3 Watts, 5%	Digi-Key#P510W-3BK-ND
R24	Metal Oxide Resistor, 510 ohms, 3 Watts, 5%	Digi-Key#P510W-3BK-ND
R25	Carbon Film Resistor, 10k, 1/4W, 5%	Digi-Key #10KQBK-ND
R26	Carbon Film Resistor, 1.1M, 1/4W, 5%	Digi-Key #1.1MQBK-ND
R27	Carbon Film Resistor, 1.1M, 1/4W, 5%	Digi-Key #1.1MQBK-ND
R28	Carbon Film Res., 10k, 1/2W, 5%	Digi-Key #10KH-ND
R29	Carbon Film Resistor, 33 ohms, 1/2W, 5%	Digi-Key #33H-ND
R30	3 Watt, non-inductive 0.1 ohms, Type LO-3-.010	Newark #96F3616
R31	3 Watt, non-inductive 0.1 ohms, Type LO-3-.010	Newark #96F3616
R32	3 Watt, non-inductive 0.1 ohms, Type LO-3-.010	Newark #96F3616
NTC 1	20 Ga (0.8mm) Jumper Wire	22 Ga Jumper
NTC 2	20 Ga. (0.8mm) Jumper Wire	22 Ga Jumper
Heatsink 1	AAVID type 61085, 1.5Deg C/W/3in., 1.5" length	AAVID #61085
Heatsink 2	Bridge Diode attachable heatsink	datogliere
PCB 1	FR-4 Material	CALS 95 001_A
T1	Coilcraft Part# R4849-A 0.5mH	CoilCraft 'Part # R4849-A
Standoffs	Aluminum Hex Standoff 0.375", 4-40 Thread	Newark#89F1949
Q1	STW20NA50, 500V, 20A, 2.7 ohms TO-247	SGS-THOMSON STW20NA50
Q2	NPN transistor high speed, 30V, .8A, TO-18 Package	SGS-THOMSON 2N2222
Q3	N-Channel Mosfet, STK2N50, 500V, 2A, SOT-82	SGS-THOMSON STK2N50
J1	3 Pole, 15A, Terminal Block	Newark #93F7182
J2	3 Pole, 15A, Terminal Block	Newark #93F7182
U1	L4981A, PFC IC	SGS-THOMSON L4981A
IC Socket	20 Pin DIP Socket, Gold Pin and Clip	Digi-Key #ED56203-ND
Misc.	Mounting screws, nuts, insulators	

Figure 2: 500W Demoboard Schematic

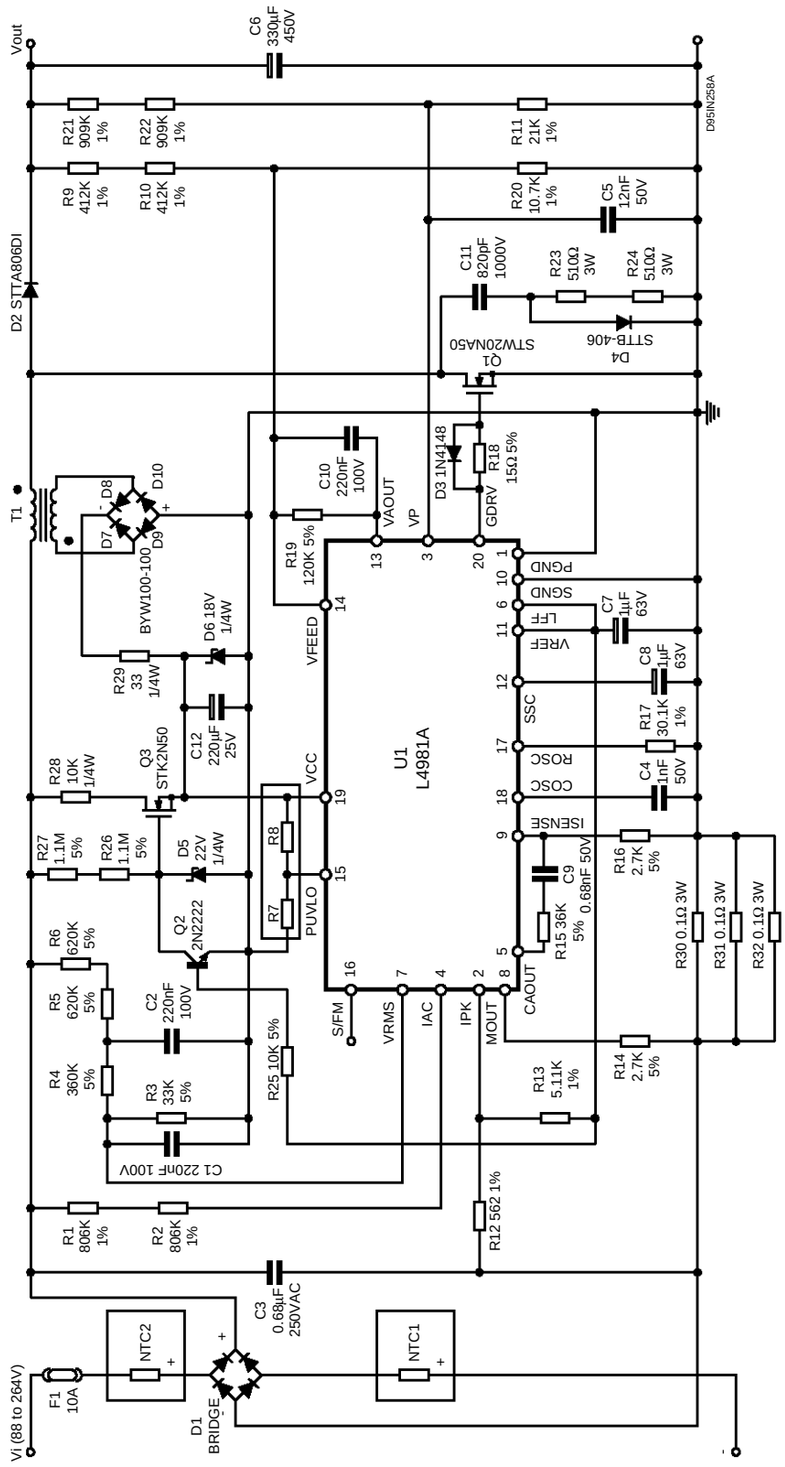
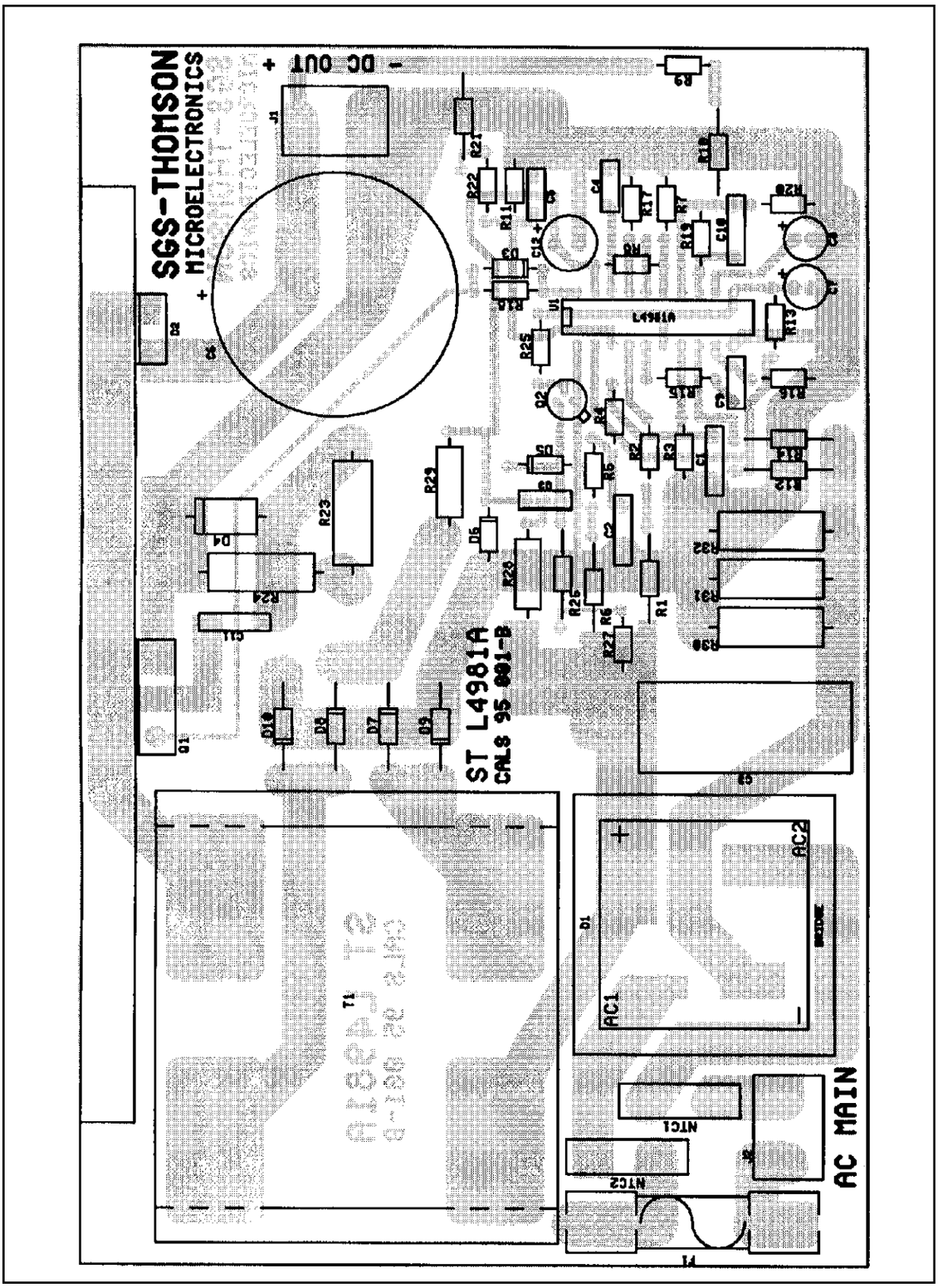


Figure 3: 500W Demoboard Printed Circuit Board Layout



An Application Program named Designing PFC [3] is available for the designer. This program allows the designer to make changes to the input/output design specifications and calculates and selects the component values and types. For example, this program can easily convert this design to single mains operation (120 or 240 Volts). The results are presented in two screens, the schematic and parts list, and may be sent to a printer for a hardcopy for future reference.

Two solutions at 110Vac (fig. 4) and 220Vac (fig. 5) are shown below.

Figure 4: 400W/230V; V_{in} =110V ±20%.

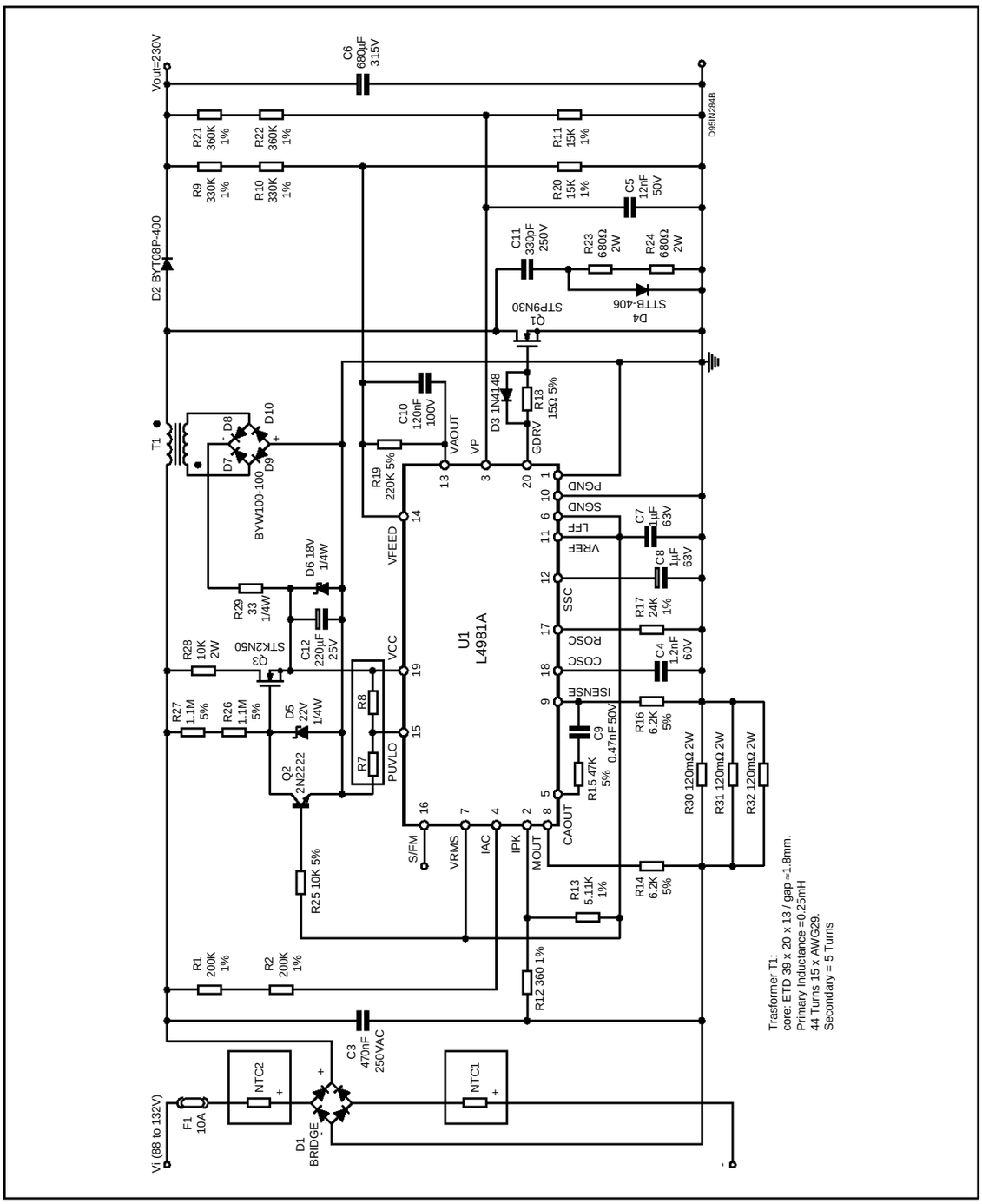
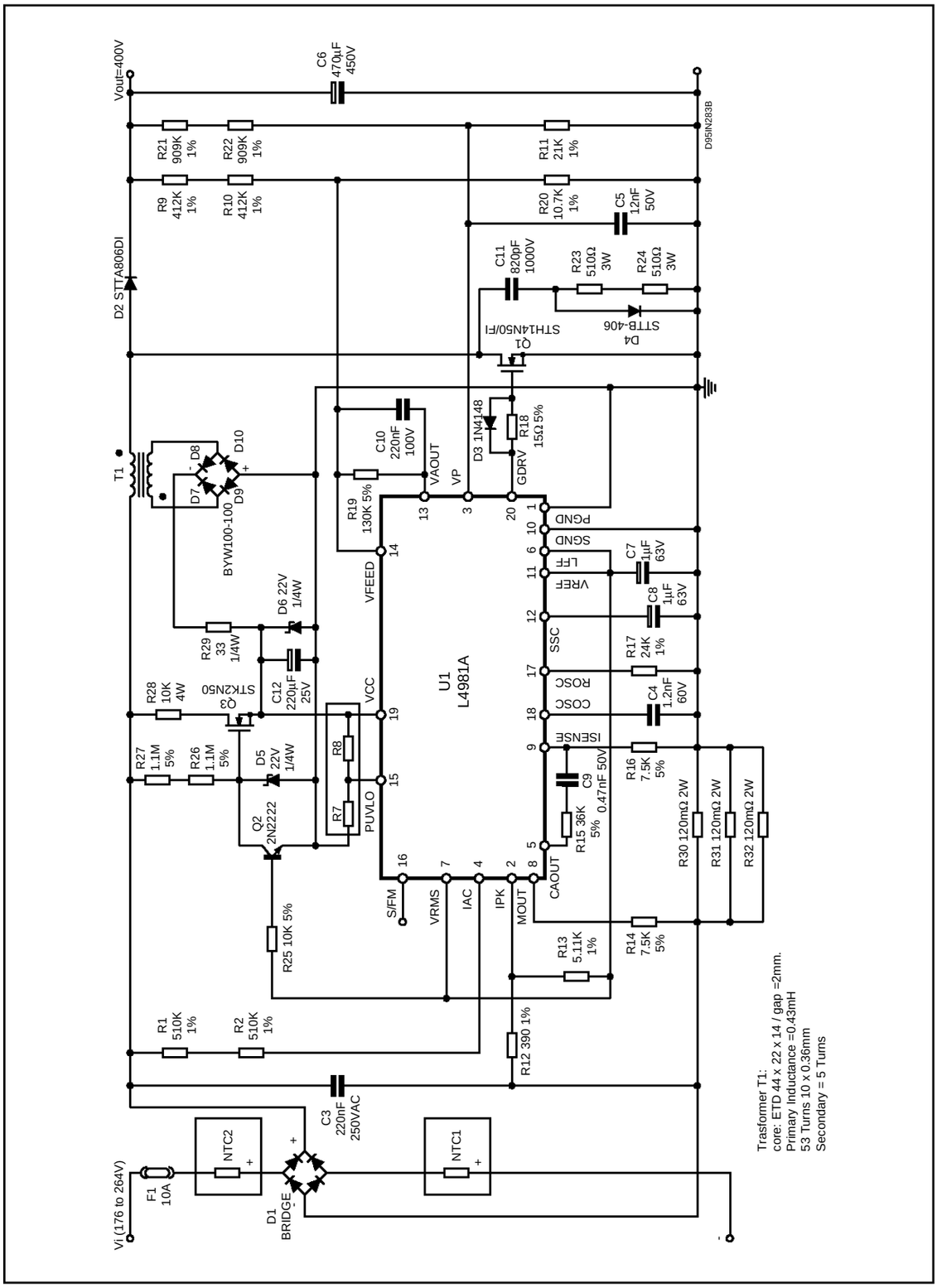


Figure 5: 800W/400V; V_{in} = 220V ±20%.



REFERENCES

[1] G. Comandatore and U. Moriconi, Application Note 628 Designing A High Power Factor Switching Preregulator With The L4981 Continuous Mode, SGS-THOMSON Microelectronics, Inc., May, 1994.

[2] Datasheet Power Factor Corrector, SGS-THOMSON Microelectronics, Inc., May, 1994.

[3] Designing PFC Application Program, SGS-THOMSON Microelectronics, Inc., April, 1995.